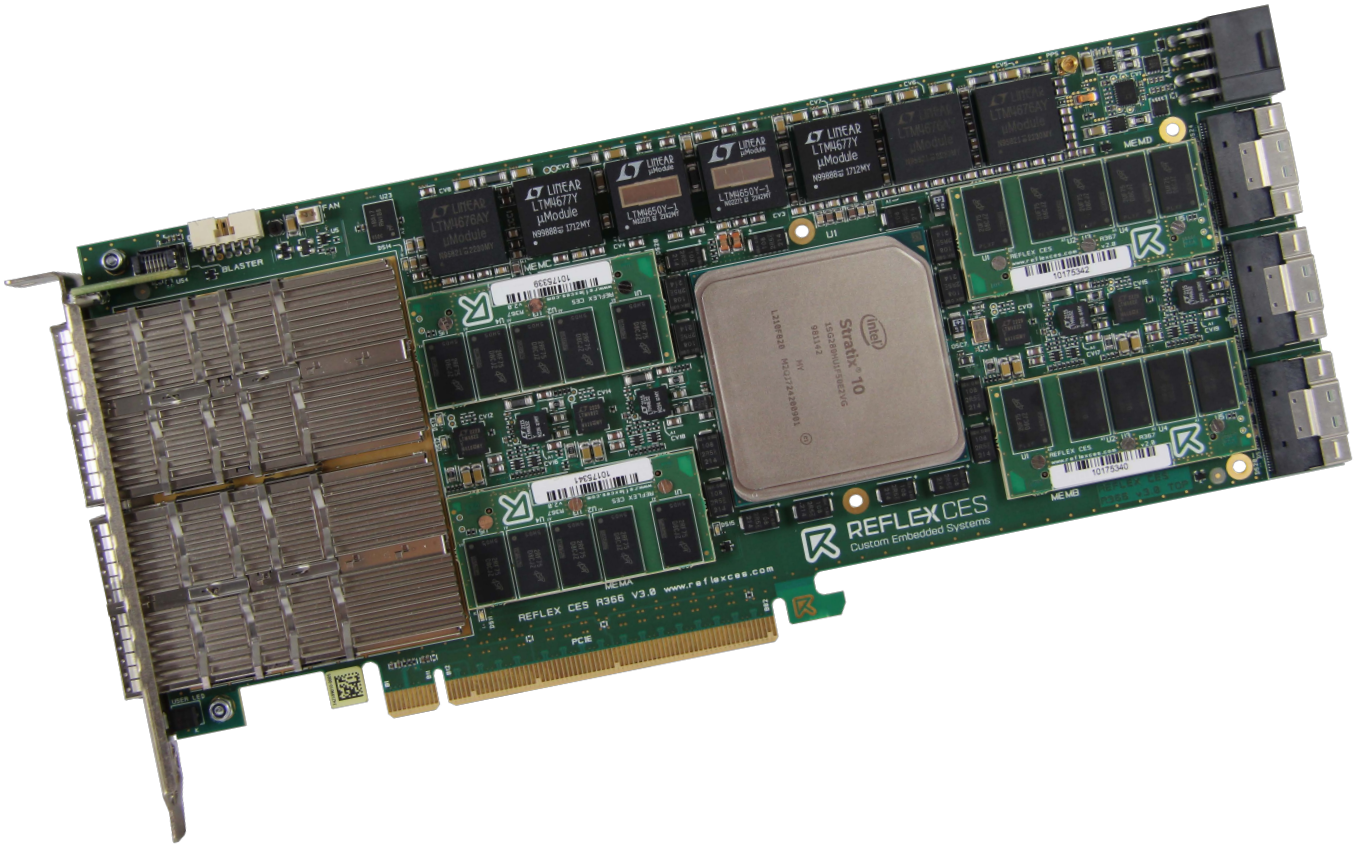
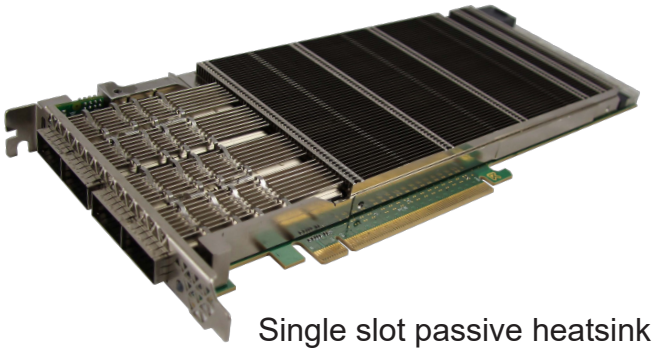
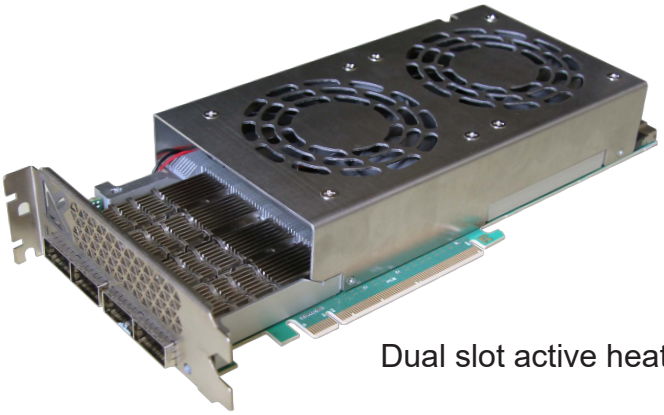
XpressGX S10-FH800G

Full height profile PCIe Network Processing FPGA board





Single slot passive heatsink



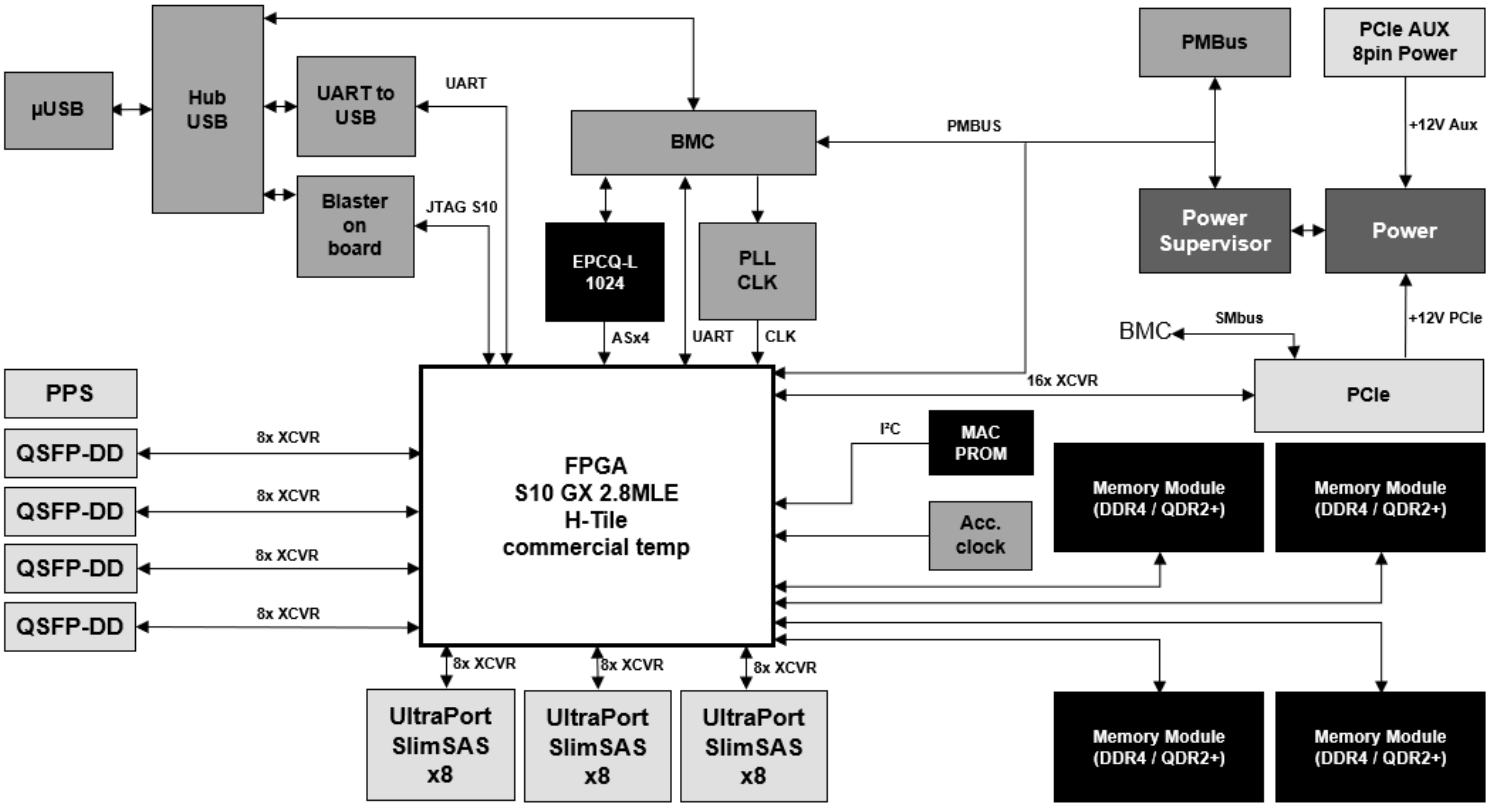
Dual slot active heatsink

Intel® Stratix® 10 GX 2800 KLE

PCIe Gen3 x16

- 4x200 GbE
- 4x DDR4 or 4x QDR2+
- Board-to-board connection

- Networking Acceleration
- Security
- High Performance Computing



Full Specifications

FPGA Configuration
- Stratix 10 GX, H-tile
- USB2.0 Micro connector for JTAG, UART and BMC
- 1x Nor Flash 1GBytes quad SPI FPGA AS configuration

Memory
- On board memory module with mix memory type DDR4 or QDRII
- 0 to 4 banks DDR4, 8GBytes each, x72bits, up to 2400MT/s
- 0 to 4 banks QDRII+ 576Mbits each, x36bits, up to 550MHz

Power
- Max 200W
- Powered by the PCIe slot and a 8-pins PCIe Aux ATX external connector (additional power)

Operating Range
0°C to 40°C

Storage Temp Range
0°C to 70°C

Board Dimensions
254mm x 111.15mm, single slot PCIe

Board Management Controller
- FPGA monitoring
- NOR Flash and clock programming

Communication Interfaces
- PCI Gen3 x16
- 4x QSFP-DD optical cage (4 x 8 XCVR : 28 Gb/s capable per XCVR link)
- QSFP-DD compatible with QSFP28 transceivers
- 3x UltraPort SlimSAS connector (NVMe interface capable, SFF-8654, 1 interface 28 Gb/s capable 8 XCVR)

Other Resources
- Programmable PLL oscillators (Si5342 & Si5344), output clocks frequency between 0.0001 MHz to 750 MHz
- High precision oscillator, clock accuracy 20MHz- 0.05ppm for Precision Time Protocol (PTP) IEEE 1588
- One coax connector for PPS (pulse per second)
- Max10 USB Blaster on board, UART over USB interface
- PMBus interface

SDK & Toolkit
The reflex cesToolkit is provided with every board purchased, to be a link between the reflex ces board and the host system. It is a suite of software development tools, including drivers, libraries, utilities and example projects.

Standards and Compliance
- RoHS/REACH compliant
- UL certified
- ISO9001 certified

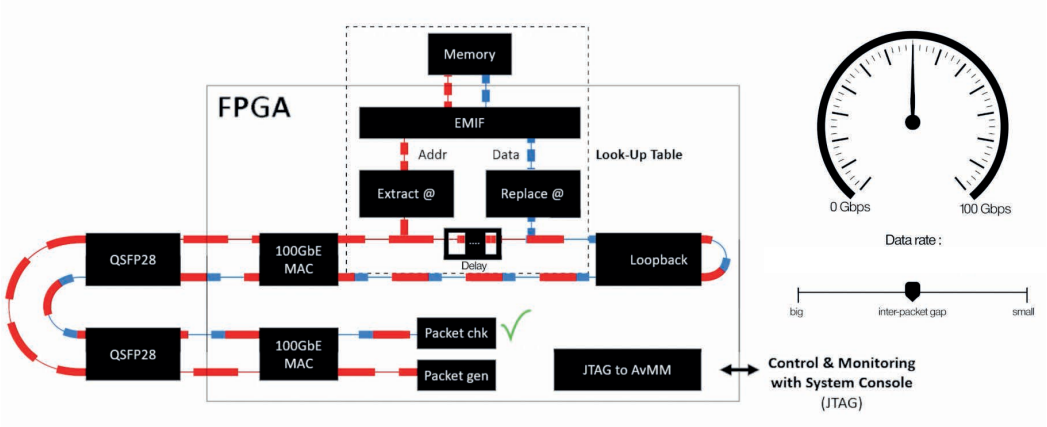
Deliverables

- Full height 1 slot PCIe board with passive heat-sink and PCIe bracket
- Board Support Package (Manuals, HDL reference designs)
- 4 memory modules DDR4 or QDRII+ (depends on the board version)
- DWF/STEP models and 2D drawing (upon request)
- LTPowerPlay project
- Online support at support.reflexces.com
- WinDriver™ PCIe device driver from Jungo

Ordering information

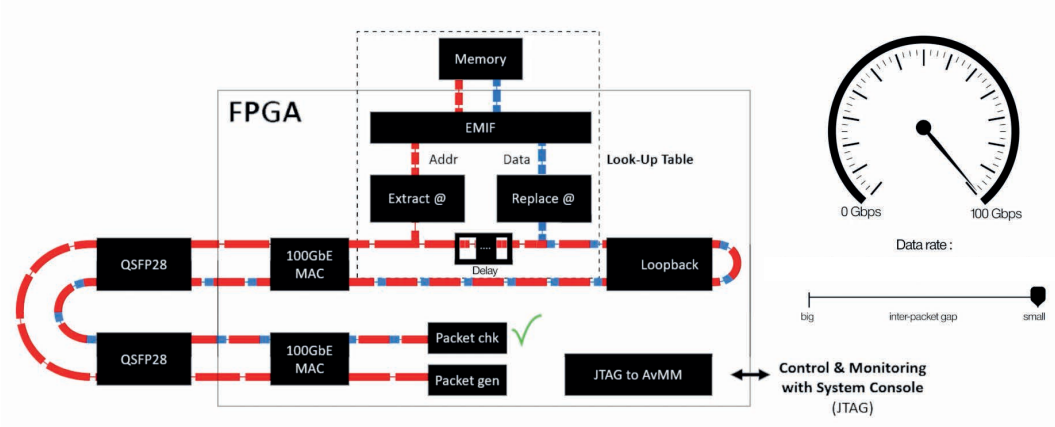
- XpressGXS10H-FH820GT = Intel Stratix 10 GX H-Tile (1SG280HU1F50E2VG), 4 banks DDR4, 1-slot PCIe passive heatsink
- XpressGXS10H-FH801GT = Intel Stratix 10 GX H-Tile (1SG280HU1F50E2VG), 4 banks QDRII+, 2-slot PCIe active heatsink
- XpressGXS10H-FH822GT = Intel Stratix 10 GX H-Tile (1SG280HU1F50E2VG), without memory, 1-slot PCIe passive heatsink

100G Ethernet packet processing Reference Design



When data rate is slow -> high inter-packet gap

Data rate increases as inter-packet gap is reduced



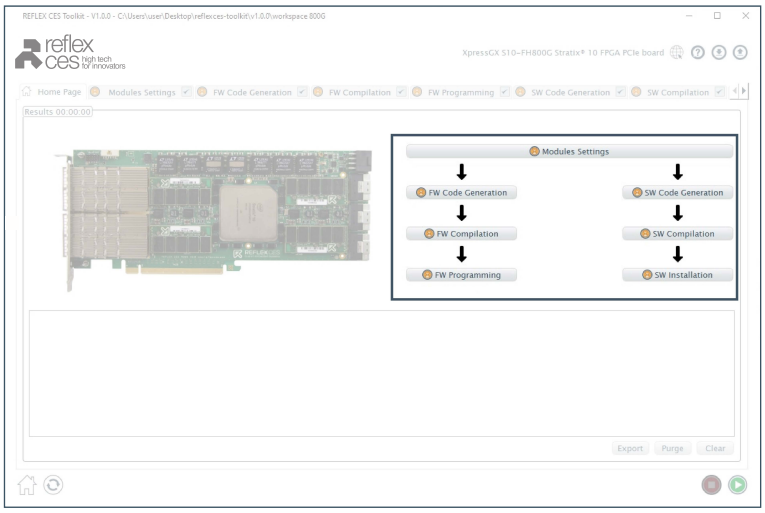
Data rate is maximum with very low inter-packet gap

100G Ethernet architecture for look-up table based packet processing

- Anti-DDoS
- IP filtering
- Bandwidth allocation

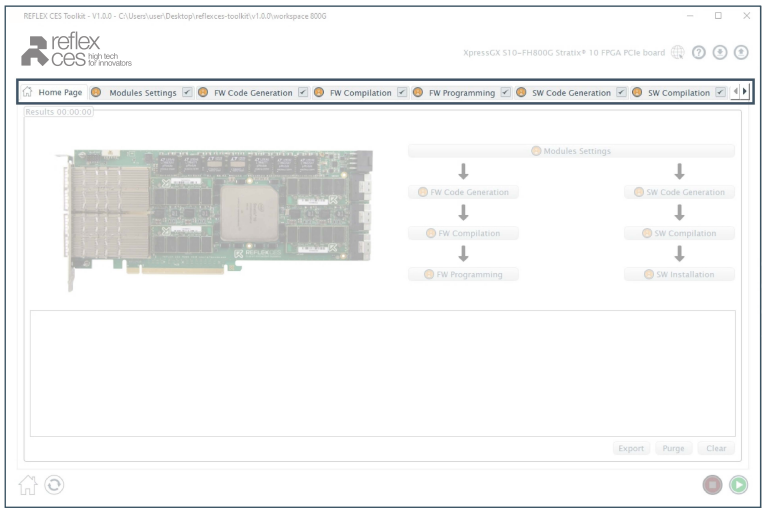
reflex ces Toolkit

The reflex ces Toolkit makes it **fast and easy** to get started with our XpressGXS10-FH800G !



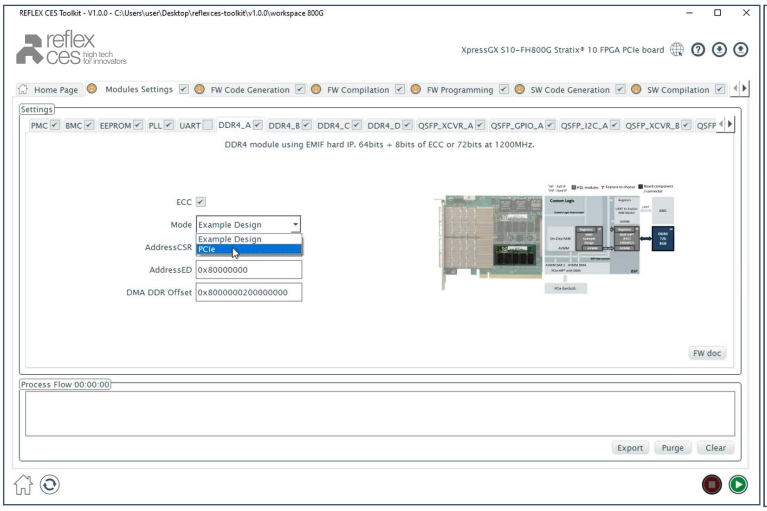
The design flow summarizes all running and deactivated tasks, and follow a logical order.

The reflex ces PCIe SDK (drivers, an API, and a test HMI provided as a software example) is included in the Toolkit.



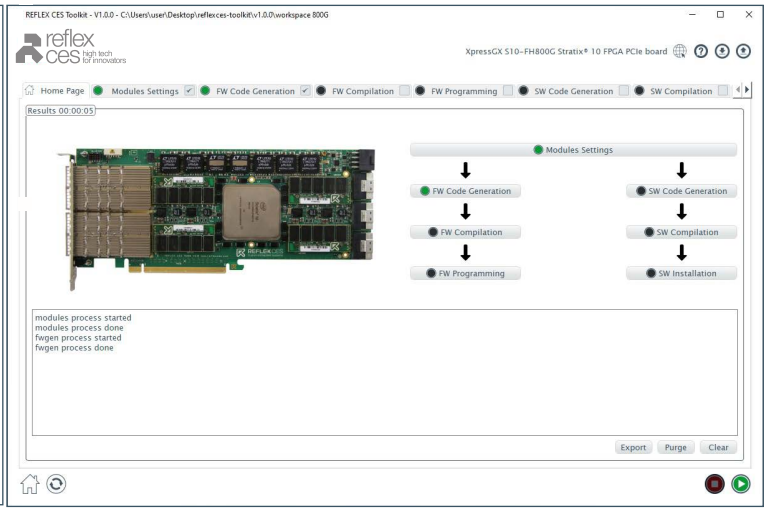
7 tasks are available on the upper banner, and can be activated and deactivated by clicking on the check box.

A page is dedicated to each task, with its specific technical information.



The generated design is fully customizable.

On the module settings tab, users can choose and configure only the interfaces required for their application.



The status of the currently running task is indicated by the color of the LED.

- Pending task
- Task completed
- Task failed

- Fully customizable Toolkit
- Fast and easy start

- Quick configuration of a design and programmation of the board, to test all the interfaces available

- Generation of a complete HDL project, including IP and test modules selected by the user through the graphical interface

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